Session 6 Overview

UWB and mm-Wave Communications Systems

Chair: *Sang-Gug Lee, ICU, Daejeon, Korea*

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Ultra wideband (UWB) systems promise a revolution in radio technology with the ability to support data rates 1Gb/s. Transceivers exemplifying two different system approaches, namely, multi-band OFDM and pulse-based schemes, continue to make significant strides in performance compared to prior years. In addition to high data-rate applications, these systems can provide highly efficient communications in terms of data-rate per unit power. The UWB approach is thus suited for wireless sensors, where the data rate is relatively modest, but battery lifetime is of critical importance. Another emerging application for UWB systems is in the area of vehicular radar. Transceivers and synthesizers for the above applications are discussed in this session.

A WiMedia-compliant UWB transceiver is discussed in Paper 6.1 by Philips and NXP Semiconductors. Implemented in a 65nm CMOS process, the highly linear transceiver supports communications in MB-OFDM band groups 1 and 3. The chip consumes 114mW by drawing 95mA from a 1.2V supply.

Paper 6.2 from Singapore Institute of Microelectronics describes a dual-band transceiver for a high-data-rate pulse-based UWB approach. The transceiver is implemented in a 0.18µm CMOS process and consumes 138.8mW in the receive mode and 99mW in the transmit mode. It supports data rates of up to 800Mb/s.

An energy-efficient receiver for wireless sensor networks is presented in Paper 6.3 by MIT. Implemented in 90nm CMOS, the radio can support data rates of up to 16Mb/s, utilizing the 3-to-5GHz UWB band with an energy requirement of 2.5nJ/b.

In Paper 6.4 from MIT, a fully digital UWB transmitter that is implemented in a 90nm CMOS process and generates PPM pulses in the 3-to-5GHz band is presented. The transmitter has a low energy requirement of 47pJ/b, and generates output pulses without using an RF oscillator.
Paper 6.5 from IMEC and Vrije U Brussel describes a low-power UWB transmitter that supports the IEEE 802.15.4a standard. It utilizes a digitally controlled oscillator to generate RF carriers for all bands between 3 and 10GHz, and a digital modulator to generate BPSK symbols at the required 500MHz chip rate.

A baseband lowpass filter for the WiMedia UWB system is presented in Paper 6.6 by TKK Helsinki. The chip uses a 5^{th}-order g_m-C lowpass topology and includes 13 to 48dB of gain control.

Paper 6.7 from USC describes a phased-array transceiver for 24GHz applications including communications and radar. The transceiver is implemented in a 0.13µm CMOS technology and uses beam-forming techniques to achieve a transmit EIRP of greater than 23.8dBm and a receiver gain that exceeds 42dB.

Finally, in Paper 6.8 from Arizona State U and TI, a 19GHz frequency-modulated continuous-wave transmitter based on a band-pass $\Delta\Sigma$ DDFS-driven RF frequency synthesizer is described. The transmitter is implemented in a 0.25µm BiCMOS process and can provide an output power of -5dBm while drawing 63mA from a 2.5V supply.

6.1 A WiMedia-Compliant UWB Transceiver in 65nm CMOS **1:30 PM**

J. Bergervoet, Philips, Eindhoven, The Netherlands

A UWB transceiver in baseline 65nm CMOS is presented. The chip has an active area of 0.4mm^2 and draws 95mA from a 1.2V supply. It achieves a NF between 5 and 5.5dB over a 3 to 8GHz bandwidth and targets MB-OFDM UWB band groups 1 and 3. The IIP3 of +5dBm and IIP2 of +24dBm make the design suitable for applications where interferer-robust operation is important.

6.2 A 0.18µm CMOS Dual-Band UWB Transceiver **2:00 PM**

Y. Zheng, Institute of Microelectronics, Singapore, Singapore

A dual-band transceiver able to work on both UWB low band (3 to 5GHz) and high band (7 to 9GHz) is presented. A method of DSB upconversion in TX, and SSB downconversion and detection in RX is proposed to achieve high data rate non-coherent communication. Realized in 0.18µm CMOS, the RX achieves an NF of 9.4dB, an IIP3 of –10.3dBm, and a sensitivity of –76dBm. It can attain a transmission rate up to 800Mb/s and draw 55mA and 76mA from a 1.8V supply in TX and RX, respectively.

6.3 A 2.5nJ/b 0.65V 3-to-5GHz Subbanded UWB Receiver in 90nm CMOS **2:30 PM**

F. Lee, A. Chandrakasan, Massachusetts Institute of Technology, Cambridge, MA

A non-coherent 0-to-16Mb/s UWB receiver using 3-to-5GHz subbanded PPM signaling is implemented in a 90nm CMOS process. The RF and mixed-signal baseband circuits operate at 0.65V. Using duty-cycling, adjustable BPFs, and an energy-aware baseband, the receiver achieves 2.5nJ/b and 10^{-3} BER with –95dBm sensitivity at 100kb/s.

6.4 A 47pJ/pulse 3.1-to-5GHz All-Digital UWB Transmitter in 90nm CMOS **3:15 PM**

D. Wentzloff, Massachusetts Institute of Technology, Cambridge, MA

An all-digital UWB TX is presented that generates PPM pulses with a center frequency tunable to 3 channels in the 3.1-to-5GHz band without the use of an RF oscillator. A delay-based spectral scrambling technique is proposed that exploits the digital architecture. The circuit achieves 47pJ/b at a data rate of 10Mb/s.

6.5 A 0.65-to-1.4nJ/burst 3-to-10GHz UWB Digital TX in 90nm CMOS for IEEE 802.15.4a **3:30 PM**

J. Ryckaert, IMEC, Leuven, Belgium and Vrije Universiteit Brussel, Brussels, Belgium

A digital UWB TX that supports the IEEE 802.15.4a standard is presented. A digitally controlled oscillator produces the RF carrier for all bands between 3 and 10GHz. It is embedded in a phase-aligned frequency-locked loop that starts up in 2ns and thus exploits the signal duty-cycle that can be as low as 3%. A digital modulator shapes the BPSK symbols at the required 500MHz chip rate. The energy requirements varies from 0.65nJ at 3.5GHz up to 1.4nJ/burst at 10GHz in 90nm 1V digital CMOS.

6.6 A 1.2V 240MHz CMOS Continuous-Time Low-Pass Filter for a UWB Radio Receiver **4:00 PM**

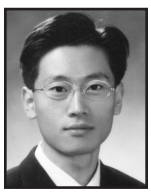
V. Saari, Helsinki University of Technology, Espoo, Finland

A 240MHz 5th-order g_m-C low-pass filter for WiMedia UWB system is presented. The filter uses a 1.2V supply and is fabricated in 0.13µm CMOS. The filter is targeted for a direct-conversion radio receiver and is based on precise-gain filter synthesis. It includes gain control from 13 to 48dB in 1dB steps. The filter achieves an input-referred noise of 7.7nV/√Hz, an out-of-band IIP3 of –8.2dBV and consumes 24mW.

6.7 A Fully Integrated 24GHz 4-Channel Phased-Array Transceiver in 0.13µm CMOS Based on a Variable-Phase Ring Oscillator and PLL Architecture **4:15 PM**

H. Krishnaswamy, University of Southern California, Los Angeles, CA

A fully integrated 24GHz 4-channel phased-array transceiver in 0.13µm CMOS is reported. The architecture is based on a variable-phase ring oscillator in a PLL that modulates the baseband for each antenna in the TX mode and downconverts the received signal from all antennas in the RX mode without using RF mixers, signal-path phase shifters, or any power combining network. The 2.3×2.1mm^2 chip achieves an array transmit EIRP >23.8dBm, RX gain >42dB, and can scan the beam continuously.



6.8 A Bandpass ΔΣ DDFS-Driven 19GHz Frequency Synthesizer for FMCW Automotive Radar **4:45 PM**

H. Chung, Arizona State University, Tempe, AZ

A 19GHz frequency-modulated continuous-wave TX based on a bandpass ΔΣ DDFS-driven RF frequency synthesizer is presented. Implemented in a 0.25µm SiGe process, the synthesizer draws 63mA from a 2.5V supply while achieving a 512MHz FM deviation with a 200Hz FM rate at a center frequency of 19GHz. The measured phase noise of the frequency synthesizer is –113.68dBc/Hz at 1MHz offset frequency from a 19GHz carrier.